CLAIMS

We claim:

1. A semiconductor memory device controlled by a memory controller, comprising:

a delay control register for receiving delay control information from the memory controller and storing the received delay control information; and

an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data,

wherein the delay time of the input buffer is controlled in response to the output signal of the delay control register.

2. The semiconductor memory device of Claim 1, wherein the input buffer comprises:

a delay controller for setting a predetermined delay time in response to the output signal of the delay control register;

a data input buffer for delaying the write data in response to the output signal of the delay controller;

an address input buffer of delaying the address signal in response to the output signal of the delay controller; and

a command input buffer for delaying the command signal in response to the output signal of the delay controller.

3. A memory controller for controlling memory modules, into which a plurality of semiconductor memory devices are loaded, comprising:

a module selector for outputting a module selection signal for selecting the memory modules in response to a clock signal;

a delay control register for receiving delay control information according to a specification from serial presence detectors (SPD) loaded into the memory modules and storing the received delay control information; and

an output buffer for delaying an internal command signal, an internal address signal, and write data in response to the output signal of the module selector and outputting the delayed write data to the semiconductor memory device,

wherein the delay time of the output buffer is controlled in response to the output signal of the delay control register.

4. The memory controller of Claim 3, wherein the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside of the memory controller.

5. The memory controller of Claim 3, wherein the module selection signal comprises:

a first signal for selecting a memory module, which does not need the predetermined delay time; and

a second signal for selecting a memory module, which needs the predetermined delay time.

6. The memory controller of Claim 5, wherein the output buffer comprises:

a delay controller for receiving the output signal of the delay control register and the second signal and setting a predetermined delay time;

a command output buffer for delaying a command signal in response to the output signal of the delay controller and the first signal;

an address output buffer for delaying an address signal in response to the output signal of the delay controller and the first signal; and

a data output buffer for delaying write data in response to the output signal of the delay controller and the first signal.

7. The memory controller of Claim 4, wherein the input buffer comprises:

a delay controller for setting a predetermined delay time in response to the output signal of the delay control register; and

a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller.

8. A memory system comprising memory modules, into which a plurality of semiconductor memory devices are loaded, and a memory controller for controlling the memory modules,

wherein the memory modules comprises SPDs for storing predetermined control information according to the specification of the memory module,

and wherein the memory controller comprises:

a delay control register for receiving the predetermined delay information from the SPDs and storing the received delay control information; and

an output buffer, whose delay time is controlled in response to the output signal of the delay control register, the output buffer for delaying a command signal, an address signal, and write data, and outputting the delayed command signal, address signal, and write data to the semiconductor memory device.

9. The memory system of Claim 8, wherein the memory controller further comprises an input buffer, whose delay time is controlled in response to the output signal of the delay control register, the input buffer for delaying read data received from the semiconductor memory device and outputting to the inside of the memory controller.

10. The memory system of Claim 9, wherein the input buffer comprises:

a delay controller for setting a predetermined delay time in response to an enable signal and the output signal of the delay control register; and

a data input buffer for delaying read data received from the semiconductor memory device and outputting the delayed read data to the inside thereof in response to the output signal of the delay controller.

11. The memory system of Claim 8, wherein the output buffer comprises:

a delay controller for receiving the output signal of the delay control register and the second signal and setting a predetermined delay time;

a command output buffer for delaying a command signal in response to the output signal of the delay controller and a first signal;

an address output buffer for delaying an address signal in response to the output signal of the delay controller and a first signal; and

a data output buffer for delaying write data in response to the output signal of the delay controller and a first signal.

12. The memory system of Claim 8, wherein each of the semiconductor memory devices comprises:

a delay control register for receiving delay control information from the memory controller and storing the received delay control information; and

an input buffer for receiving a command signal, an address signal, and write data from the memory controller and delaying the received command signal, address signal, and write data,

wherein the delay time of the input buffer is controlled in response to the output signal of the delay control register.

13. The memory system of Claim 12, wherein the input buffer comprises:

a delay controller for setting a predetermined delay time in response to the output signal of the delay control register;

a data input buffer for delaying the write data in response to the output signal of the delay controller;

an address input buffer for delaying the address signal in response to the output signal of the delay controller; and

a command input buffer for delaying the command signal in response to the output signal of the delay controller.

14. A method for controlling the delay time of an input signal input to a semiconductor memory device controlled by a memory controller, comprising the steps of:

receiving delay control information from the memory controller and storing the received delay control information;

setting a predetermined delay time in response to the stored delay control information; and

controlling the delay time of a signal input to the semiconductor memory device by the predetermined delay time.

15. The method of Claim 14, wherein the input signal is a command signal, an address signal, and write data.

16. A method for controlling the delay time of the output signal of a memory controller output to memory modules, into which a plurality of semiconductor memory devices are loaded, comprising the steps of:

receiving delay control information according to the specification of the memory modules from SPDs loaded into the memory modules and storing the received delay control information;

outputting a module selection signal for selecting the memory modules in response to a clock signal;

setting a predetermined delay time in response to the stored delay control information and a first signal; and

controlling the delay time of the output signal output to the semiconductor memory device by the delay time.

17. The method of Claim 16, wherein the method for controlling the delay time further comprises the step of controlling the delay time of a signal input from the semiconductor memory device to the memory controller by the delay time.

18. The method of Claim 16, wherein the output signal is a command signal, an address signal, and write data.

19. The method of Claim 16, wherein the module selection signal comprises:

a first signal for selecting a memory module, which does not need the predetermined delay time; and

a second signal for selecting a memory module, which needs the predetermined delay time.

20. A method for controlling the delay time of a signal between memory modules, into which a plurality of semiconductor memory device are loaded, and a memory controller for controlling the memory modules, comprising the steps of:

receiving delay control information according to the specifications of the memory modules from SPDs loaded into the memory modules and storing the received delay control information;

outputting a module selection signal for selecting the memory modules in response to the clock signal;

setting a predetermined delay time in response to the stored delay control information and a first signal;

outputting the delay control information to the semiconductor memory device by the delay time;

receiving the delay control information from the memory controller and storing the received delay control information;

setting a predetermined delay time in response to the stored delay control information; and

controlling the delay time of a signal input to the semiconductor memory device by the predetermined delay time.

21. The method of Claim 20, wherein the signal is a command signal, an address signal, and write data.

22. The method of Claim 20, wherein the delay time further comprises the step of controlling the delay time of a signal input from the semiconductor memory device to the memory controller by the predetermined delay time.

23. The method of Claim 20, wherein the module selection signal comprises:

a first signal for selecting a memory module, which does not need the predetermined delay time; and

a second signal for selecting a memory module, which does not need the predetermined delay time.

24. An integrated circuit memory system, comprising:

a plurality of memory modules, a respective one of which being responsive to a control signal and having delay control information stored thereon; and

a memory controller that is configured to generate the control signal in response to the delay control information.

25. The integrated circuit memory system of Claim 24, wherein the memory controller further comprises:

a delay control register that is configured to receive and to store the delay control information therein; and

an output buffer that is configured to generate the control signal in response to an input control signal and the delay control information stored in the delay control register.

26. The integrated circuit memory system of Claim 25, wherein each of the plurality of memory modules has delay control information stored thereon, and wherein the delay control information comprises a transmission delay value between the memory controller and the respective memory module, the integrated circuit memory system further comprising:

a delay controller that is configured to generate a delay signal in response to an activated select signal and to the delay control information stored in the delay control register, the output buffer being responsive to the delay signal; and

a module selector that is configured to deactivate the select signal if the transmission delay value associated with the respective one of the plurality of memory modules is greater than or equal to the transmission delay values associated with the other ones of the plurality of memory modules.

27. The integrated circuit memory system of Claim 25, wherein the memory controller further comprises:

an input buffer that is configured to receive data from the respective one of the plurality of memory modules at an input thereof and to provide the received data at an output thereof in response to the delay control information stored in the delay control register.

28. The integrated circuit memory system of Claim 25, wherein the control signal comprises a command control signal, an address control signal, and data, and wherein the output buffer comprises a command output buffer that is configured to

generate the command control signal in response to an input command control signal and the delay control information stored in the delay control register, an address output buffer that is configured to generate the address control signal in response to an input address control signal and the delay information stored in the delay control register, and a data output buffer that is configured to generate the data in response to input data and the delay information stored in the delay control register.

29. The integrated circuit memory system of Claim 24, wherein at least one of the plurality of memory modules comprises a plurality of memory devices.

30. The integrated circuit memory system of Claim 29, wherein the control signal is a first control signal, and wherein a respective one of the plurality of memory devices comprises:

a delay control register that is configured to receive at least some of the delay control information and to store the at least some of the delay control information therein;

an input buffer that is configured to generate a second control signal in response to the first control signal and the delay control information stored in the delay control register; and

a memory cell array that is responsive to the second control signal.

31. An integrated circuit memory device, comprising:

a delay control register that is configured to receive delay control information and to store the delay control information therein;

an input buffer that is configured to generate a control signal in response to an input control signal and the delay control information stored in the delay control register; and

a memory cell array that is responsive to the control signal.

32. The integrated circuit memory device of Claim 31, further comprising:

a delay controller that is configured to generate a delay signal in response to an enable signal and the delay control information stored in the delay control register, the input buffer being responsive to the delay signal.

33. The integrated circuit memory device of Claim 31, wherein the control signal comprises a command control signal, an address control signal, and data, and wherein the input buffer comprises a command input buffer that is configured to generate the command control signal in response to an input command control signal and the delay control information stored in the delay control register, an address input buffer that is configured to generate the address control signal in response to an input address control signal and the delay information stored in the delay control register, and a data input buffer that is configured to generate the data in response to input data and the delay information stored in the delay control register.

34. A memory controller for use in a memory having a memory module, the memory controller comprising:

a delay control register that is configured to receive and to store delay control information associated with the memory module therein; and

an output buffer that is configured to generate a control signal for the memory module in response to an input control signal and the delay control information stored in the delay control register.

35. The memory controller of Claim 34, further comprising:

an input buffer that is configured to receive data from the memory module and to provide the received data at an output thereof in response to the delay control information stored in the delay control register.

36. The memory controller of Claim 34, wherein the delay control information comprises a transmission delay value between the memory controller and the memory module, the memory controller further comprising:

a delay controller that is configured to generate a delay signal in response to an activated select signal and to the delay control information stored in the delay control register, the output buffer being responsive to the delay signal; and

a module selector that is configured to deactivate the select signal in response to the transmission delay value.

37. The memory controller of Claim 34, wherein the control signal comprises a command control signal, an address control signal, and data, and wherein

the output buffer comprises a command output buffer that is configured to generate the command control signal in response to an input command control signal and the delay control information stored in the delay control register, an address output buffer that is configured to generate the address control signal in response to an input address control signal and the delay information stored in the delay control register, and a data output buffer that is configured to generate the data in response to input data and the delay information stored in the delay control register.

38. A method of operating an integrated circuit memory system comprising a memory controller and a plurality of memory modules, the method comprising:

receiving delay control information associated with one of the plurality of memory modules at the memory controller;

delaying a control signal based on the delay control information; and

transmitting the delayed control signal from the memory controller to the one of the plurality of memory modules.

39. The method of Claim 38, wherein receiving delay control information associated with one of the plurality of memory modules at the memory controller comprises receiving delay control information respectively associated with each of the plurality of memory modules at the memory controller, and wherein the delay control information comprises a transmission delay value between the memory controller and the respective memory module.

40. The method of Claim 39, wherein delaying the control signal based on the delay control information comprises:

applying a non-zero delay to the control signal if the transmission delay value associated with the one of the plurality of memory modules is less than at least one of the transmission delay values associated with other ones of the plurality of memory modules.

41. The method of Claim 38, further comprising:

receiving data from the one of the one of the plurality of memory modules at the memory controller;

storing the received data in an input buffer; and

providing the received data at an output of the input buffer after a delay time period that is based on the delay control information has elapsed.

42. The method of Claim 38, wherein at least one of the plurality of memory modules comprises a plurality of memory devices, and wherein the delayed control signal is a first control signal, the method further comprising:

receiving at least some of the delay control information from the memory controller at a respective one of the plurality of memory devices;

delaying the first control signal based on the at least some of the delay control information; and

providing the delayed first control signal to the memory cell array

43. A method of operating an integrated circuit memory device that comprises a memory cell array and is communicatively coupled to a memory controller, the method comprising:

receiving delay control information from the memory controller at the memory device;

delaying a control signal based on the delay control information; and

providing the delayed control signal to the memory cell array.

44. The method of Claim 43, wherein delaying the control signal, comprises:

receiving the control signal from the memory controller at the memory device.